(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 739 039 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
23.10.1996 Bulletin 1996/43

(51) Int. Cl.[6]: **H01L 27/146**

(21) Application number: **96870050.0**

(22) Date of filing: **18.04.1996**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB IE IT LI NL SE

(30) Priority: **18.04.1995 EP 95870037**
12.05.1995 EP 95870053

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(54) Pixel structure, image sensor using such pixel, structure and corresponding peripheric circuitry

(57) A pixel (100 or 500) structure for CMOS imaging applications, comprising:

- a photosensitive element (10 or 50)
- a load transistor (11 or 51) in series with the photosensitive element (10 or 50);
- means comprising at least another transistor (13, 14 or 22, 23 or 32 or 53) coupled to said photosensitive element (10 or 50) and said load transistor (11 or 51) for reading out the signals acquired in said photosensitive element (10 or 50) and converting to a voltage drop across said load transistor (11 or 51), characterized in that the gate length of at least the load transistor (11 or 51) is increased by at least 10% compared to the gate length of the transistors manufactured according to the layout rules imposed by CMOS manufacturing process, whereby increasing the light sensitivity of said pixel structure.

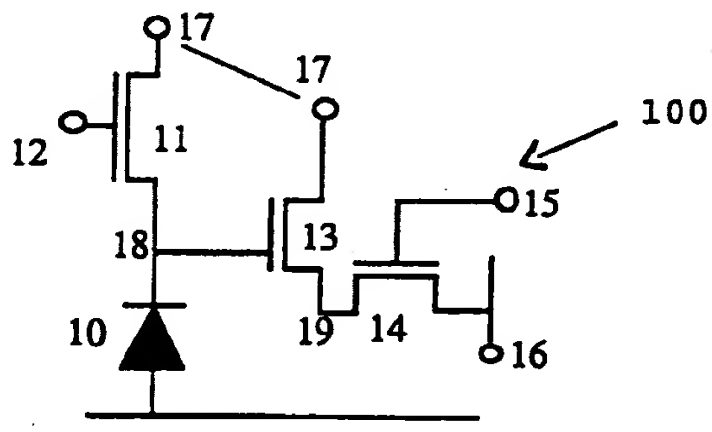

fig. 2

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Description

Object of the Invention

The present invention relates to a pixel structure for imaging application, to CMOS image sensors using such pixel structure and to the corresponding peripheric circuitry.

Background of the Invention

CCD-based cameras are commonly used as input devices for image analysis systems. A disadvantage of this class of devices is that when real-time operation is required, only essentially simple calculation can be performed on the CCD output data stream.

Document US-A-5 335 008 is directed to a CCD image sensing device in which an amplifying transistor for amplifying a photoelectrically-converted signal charge and outputting the amplified signal charge to a vertical signal line is provided at every pixel of a plurality of pixels arrayed in a two-dimensional fashion and wherein a load transistor is connected to each of the vertical signal lines, in which the load transistor is composed of a first field effect transistor having a constant current characteristic and a second field effect transistor acting as a negative feedback resistor function connected in series.

In this description, it is the first MOSFET transistor which is reacting as the load of a signal line and serving therefore as the load of a source follower. Accordingly, this transistor has no direct relation with the signal read from the photodiode.

Furthermore, this document describes a CCD image sensing device wherein the first MOSFET transistor has a large ratio W/L wherein W is its channel width and L is its channel length.

However, it should be noted that such W/L ratio affects directly the gate voltage (V_G - V_{th}) of the MOSFET for a given current. The aim of precising this characteristic is to suggest to have a linear resistance using MOSFET transistors. Accordingly to reach such linear operation it is necessary to work in the "$V_G > V_{th}$" region.

CMOS based flexible imaging sensors have been developed recently (S. Anderson, IEEE 1991, Custom Integrated Circuits Conference, pp. 12.1.1-12.1.4). Examples of these sensors include the IMPUTER of the company VLSI Vision Ltd. (Scotland) and the product MAP2200 of Integrated Vision Products (Sweden).

Document EP-A-0 548 981 is describing a classic image sensor of the integrating type and having a particular source follower circuit. Each pixel in this image sensor comprises one MOSFET of a complex nature so that it includes light sensitive means. In this device, the photo current is accumulated on a capacitance and grows during elimination. At the end of "integration time", it must be reset. The same principle is found in many diode arrays, CCD's devices, MOSFET camera, etc.

Document WO93/19489 describes an imaging chip intended to be use in a CMOS image sensor with a large number of image pixels are provided with field-effect transistors and a read-out logic. In order to map a high input signal dynamic ratio onto a reduced output signal dynamic ratio, each image pixel is connected to one electrode of a first MOS transistor and to the gate of a second MOS transistor while the other electrode of the first MOS transistor is connected to one pole of a voltage source.

The reference Microelectronics Engineering 19 (1992) pp. 631-634 discloses an image array of 256 by 256 pixels developed in a 2.4 micron CMOS technology. Said array acts as an asynchronous component having as control signals of one pixel, two 8 bit input words forming the address of said pixel and one analog output. This device is fully addressable which implies that the pixels can be read out in a true random sequence. Furthermore, the pixels can be read out instantaneously, which is a consequence of the fact that in the chosen device architecture the detected photocurrent is continuously converted to a low impedance voltage signal within the pixel. A general view of the device architecture will be described in detail in the sequel and more particularly in connection with figures 1 and 2.

The device described in such a document has a use as a compact, low cost smart vision sensor, e.g. for industrial imaging purposes. The device concept allows cointegration with digital logic, in order to build smart vision cameras. The logarithmic response causes this sensor to respond to a broad range of illumination conditions, with nearly perfect anti-blooming performance.

The combination of the addressability and continuous, asynchronous readout characteristics allow to read out the response of any pixel any time. Both characteristics are intimately linked, adaptations in device architecture to improve one of both aspects have a direct advantageous leverage effect on the other (addressability or continuous read-out) characteristic.

It is evident that using the above described technology, one can achieve a sensor having either addressability characteristics or continuous readout characteristics.

Problem definition

The CMOS image sensor as disclosed in the above-mentioned reference shows apparent shortcomings for applications such as industrial imaging. The main disadvantage of the circuit as described in the prior art and currently on sale is that the quality of the image is inferior to the one of high-end CCD systems.

More particularly, it is a first disadvantage of the circuit as described in the prior art and currently on sale is that the light sensitivity of the imaging device is limited by constraints inherently linked with the implementation in the CMOS technology.

It is a second disadvantage of the circuit as described in the prior art and currently on sale is that an absolute measure of the light intensity cannot be provided due to the chosen device architecture.

It is a third disadvantage of the circuit as described in the prior art and currently on sale is that a brightness control of the image cannot be achieved by state-of-the-art techniques applied for CCD's or for imaging devices based on integrating techniques.

It is a fourth disadvantage that the homogeneity of the image is inherently degraded by the statistical spread on the individual pixel characteristics. Defective "white pixels" can degrade the image homogeneity as well.

It is a fifth disadvantage that all the sensors described hereabove have only black and white contrast and accordingly, no color sensitivity.

Summary of the Invention

The aim of the present invention is to disclose new devices that overcome the drawbacks of the device and the circuit disclosed in the prior art.

The present invention relates to a pixel structure for CMOS image sensors comprising a photosensitive element, a load transistor in series with the photosensitive element and means, comprising at least another transistor, coupled to said photosensitive element and said load transistor for reading out the signals acquired in said photosensitive element and converting it to a voltage drop across said load transistor. The present invention is essentially characterized by the fact that the gate length of at least the load transistor is increased by at least 10% compared to the gate length of transistors manufactured according to the layout rules imposed by the CMOS manufacturing process.

According to one preferred embodiment, such structure can be realised in one individual pixel, and in such case, a CMOS image sensor will be achieved with a geometric configuration of a (j x k) matrix of pixels, each pixel having a photodiode, a load transistor and read-out means.

According to one preferred embodiment, each pixel of the CMOS image sensor has at least one photodiode and a load transistor of which the drain is not tied to a voltage supplier and wherein the read-out means comprise at least a second transistor and a third transistor which is directly connected to the data read-out line.

According to another preferred embodiment, each pixel of the CMOS image sensor has only one photodiode and two transistors among them a load transistor and another transistor connected to the data read-out line. Said pixel can be read-out in both X - Y and Y - X modes.

According to another preferred embodiment, one pixel comprises only a photodiode and a switch since the load transistor and the read-out means are common for several pixels.

Other characteristics and advantages are described hereunder.

Brief Description of the Drawings

Figure 1: is a schematic view of the architecture of a CMOS image sensor according to the state of the art.

Figure 2: is a schematic representation of the pixel structure as described in the state of the art and used in the sensor described in figure 1.

Figure 3: is a measured graph representing the logarithmic value of the current through a MOSFET transistor (log(I)) versus the voltage (V), for different lengths of the MOSFET's gate for two precise embodiments of a pixel structure wherein the gate length is [10 μm x 0.25 μm] and [10 μm x 0.5 μm] respectively.

Figures 4 & 5 represent two other preferred embodiments of the new configuration for pixels structure for a CMOS sensor according to the present invention.

Figure 6: represents another preferred embodiment of a configuration of pixels for a CMOS sensor according to the present invention.

Figure 7: represents one implementation for a group of 2 x 2 pixels according to another preferred embodiment of the present invention.

Figure 8: represents a schematic view of the peripheric circuit controlling the brightness for an image sensor according to the present invention.

Figure 9: represents the responses of the light intensity (A) versus the sensor output voltage (V) for different stress conditions.

Figure 10: represents a camera using the electronic image sensor according to the present invention.

Figure 11: represents a flow sheet for the fabrication method of a color filter which will be laid on an image sensor according to the present invention.

Detailed Descriptions of Several Preferred Embodiments of the Invention

A general view of a CMOS image sensor is described in figure 1, wherein (1) represents one pixel array surrounded by dummy pixels, (2) represents row selection circuits, (3) represents buffers, (4) represents load transistors for the readout lines, (5) represents emitter follower transistors and multiplexers for the output voltages, (6) represents column selection circuits,

(7) represents the output structure, (8 & 9) represent address input buffers. In operation, a row selection circuit selects one row of the array, putting the corresponding signals on vertical readout lines. The column selection circuit (6) selects one of the emitter followers, leading in that way the signal of one pixel to the output.

In the following lines, for the purpose of the teaching of the invention, an implementation of the imaging sensor as a 512 x 512 active pixel CMOS imager is assumed. Each pixel contains one photodiode and 3 MOSFET transistors, and has a pitch of 6.6 micrometer using a 0.5 micrometer CMOS technology.

The total number of transistors in the CMOS imaging sensor of the present embodiment amounts up to 808000. The fill factor can be only 15%. The small photosensitive area of this type of pixels (compared to the integrating type of imagers) does not degrade speed performance. The nominal supply voltage is 3.3 V, but it appears to work with no degradation between 1.7 V and 5 V.

Figure 2 gives a schematic representation of the structure of a pixel (100) used in the device described in figure 1. Light is converted into a photodiode current (photodiode (10)) flowing through a load transistor (11). This current is in the order of femtoamperes to nanoamperes. Thus, the load transistor (11) operates in weak inversion, also called sub-threshold mode ($V_G << V_{th}$) and as a consequence the photocurrent to voltage transition is logarithmic dependent on the current. The source voltage (12) of the load transistor (11) is buffered by an emitter follower (transistor 13). A selection transistor (14) of the pixel is connected to an activating line (15) and a data readout line (16).

Thus, a fully addressable pixel matrix (1) with direct current sensing pixels (100) as described in figure 2 and having a logarithmic response is disclosed. in said reference.

It is a first object of the present invention to provide a new pixel and a CMOS image sensor having improved light sensitivity. This means improved quality of the light/voltage conversion. The sensitivity of the pixel disclosed in the state of the art at low light intensities may be limited by the leakage current through the load transistor (11).

In figure 3, curve a shows the logarithm of the current (Log(I)) trough the load transistor (11) as a function of voltage V. On this figure, one can see that at lower currents, the voltage over the transistor (11) is near zero and does not vary significantly.

To overcome this limitation, the gate length of transistors and more particularly of the load transistor (11) is increased by at least 10% compared to the gate length of transistors manufactured according to the layout rules of the CMOS manufacturing process. The gate length of the transistors such as the load transistor (11) is usually dictated by the requirements of the minimum area occupation and is imposed by the layout rules used for a specific CMOS manufacturing process advised by the silicon foundry. Such CMOS manufacturing process can be a 0.7 μm, 0.6 μm, 0.5 μm, 0.25 μm, 0.18 μm manufacturing process, or any other conventional manufacturing process known by the man skilled in the art.

A specific CMOS manufacturing process is defined by specific rules according to which devices such as CMOS image sensors can be fabricated.

These rules comprise prescriptions for implementation of successive layers wherein thickness of oxides, diffusion time, and other characteristics known by the man skilled in the art are precisely followed.

An important and more cited characteristic is also the characteristic defining the minimum dimension of the gate length of the transistors manufactured by such process.

Therefore, for instance for a 0.5 μm CMOS manufacturing process, the transistors are designed with a gate length of 0.5 μm. This characteristic is therefore referred to in the sequel as the layout rules imposed by a specific CMOS manufacturing process.

For instance if transistors (such as transistors 13 & 14 of Figure 2) have a gate length of 0.5 μm, this means that they are fabricated by the 0.5 CMOS manufacturing process.

In this case, according to the present invention, at least the load transistor (11) should show a gate length of at least 0.55 μm.

As a result of this characteristic, the load transistor (11) in figure 3 shows a saturation at lower current densities.

An increased sensitivity of the pixel for lower light intensities (current densities) is apparent. The saturating regime in curve a is caused by the "punch through" phenomenon in the weak inversion region of MOS transistors. By increasing the gate length, a geometrical separation of source and drain regions is obtained, and the leakage current decreases. An increase of the sensitivity by a factor of 10 to 100 is realized.

Figure 3 is representing two examples of measurements done for two pixel structures as represented in figure 2, wherein the value [W x L] is [10 x 0.25 μm] and [10 x 0.5] μm respectively. Accordingly, in this figure wherein an increase of the gate length of 100% is represented, one can observe the sensitivity is increased by a factor of at least 4 decades.

Figure 4 is describing another preferred embodiment of a pixel structure according to the present invention which shows also a logarithmic response. This pixel has the main characteristics of the present invention and includes a photodiode (10), a load transistor (11) in series with the photodiode as well as read-out means (22 and 23).

However, in this case, the drain of the load transistor (11) is not directly tied to the output signal supply. The read-out means consist in a second MOSFET (22) which is not a source follower and finally, a third MOSFET (23) which acts as a switch. A current source (24) is providing the current of the order of microamperes. The gate of the transistor (23) is tied to the address.

While the photodiode (10) can be considered as also a current source (of the order of femtoamperes to nanoamperes according to the intensity of light impinging the photodiode) the transistor (23) is conducting the current decharging through the transistor (22). Such current can be defined by:

$$I_2 \sim c\,(V_G - V_{th})$$

wherein c is a constant value.

As I_2 is given by the current source and is more or less a constant, we have then V_G also nearly a constant.

Therefore, the light acquired by the photodiode (10) is converted into a voltage drop across the load transistor (11).

This pixel has accordingly the equivalent functions as the one described in figure 2. Alternatively, this pixel can be also considered as a simple and classic resistive feedback amplifier.

Figure 5a and 5b describe a pixel structure for a CMOS sensor using only two MOSFETs (11 and 32) which can be read out in both X - Y (fig. 5a) and Y - X modes (fig. 5b). Since this array has X - Y interchangeability, one can choose to have addressing high speed in either X - or Y - directions which can be relevant for particular applications.

According to the X - Y mode described in fig. 5a, one can apply high voltage to the row to be addressed (36) while low voltage is applied to load column bus to ground (37).

According to the Y - X mode represented in fig. 5b, one can apply low voltage to the column to be addressed (38) and high voltage to the load row bus to VDD supply (39).

Using the same imaging area, one can increase the optical resolution using the pixel structure as described in figure 6.

According to such configuration, one pixel comprises only a photodiode (50) and a switch (54) while the load transistor (51) and the read-out means (53) are common to one unit of pixels (500), a unit being e. g. a column or a row of pixels.

It is a further object of the present invention that an electronic circuit is provided by which an absolute measurement of the light intensity is realized. Hereto, a pseudopixel (not represented) which does not have an imaging function is integrated in the imager as disclosed in figure 1. In said pseudopixel, the photodiode (10) is replaced by current sources integrated in the chip according to techniques known by those skilled in the art. A known current density is generated by said current sources. The output voltage of said pseudopixel is compared to the output voltage of pixels containing a photodiode. In order to determine the absolute light intensity on these pixels, which is proportional to the photocurrent and an independent calibration has still to be performed to determine the proportional coefficient between the light intensity and the photocurrent.

It is a further object of the present invention that an electronic circuit is provided wherein certain error signals, known as so-called "white pixels" are corrected by an averaging or minimization operation on a group of pixels in the same area. An implementation is shown in figure 7. A group of 4 pixels (70) (71) (72) (73) is treated as one group for signal processing. According to the implementation shown, a kind of minimum or average value or minimized value of the 4 pixels will be used for further processing. In case one of the pixels, assume pixel (70), has a defective, e.g. leaking photodiode, in the addressing of the pixel, switches (74) and (75) will be closed and the output signal of pixel (70) will be replaced by an appropriate average value of the pixels (71) (72) and (73). It is evident that any other implementation of such correction method can be imagined. Any (m x n) group of pixels within the pixel matrix will lead to the same result if some kind of averaging or minimization operation is performed and if the extreme values which arise from defective pixel(s) are disregarded.

It is a further object of the invention that an electronic circuit is provided, with a built-in automatic control of the brightness of the image. Figure 8 represents a sensor, according to the present invention, wherein the output voltage (80) of the pixel matrix (800) receives an offset correction before it is applied as an input voltage (82) to a signal processing unit, e.g. an Analog-to-Digital-Convertor (ADC) (83). Hence, the output voltage (80) can be brought within the required range of input voltages of the ADC (83). By means of a control circuit (84) with a lowpass filter transfer function (85), the output voltage (80) is increased or decreased until the input voltage (82) at the ADC (83) is within the selected range of the ADC (83). The correction on the output voltage (80) is given by a circuit (85) which yields a slowly varying voltage. This correction circuit acts as an automatic brightness regulating instance for the sensor (81).

It is a further object of the present invention that an electronic circuit is provided in which on chip a non-uniformity correction is realized. Non-uniformities in the read-out characteristics of the different pixels arise from the statistical spread on the threshold voltage (V_{th}) of the transistors (11-14) and photodiode (10) in the matrix. For each pixel, the actual non-uniformity is the sum of three V_{th} distributions. The situation is especially unfavorable in the case when these transistors have submicron effective sizes which enhance the geometry dependant non-uniformity. For an acceptable image quality, the output signal must be offset corrected pixel by pixel, e.g. by using an external frame memory or by software. This jeopardizes the possibility of self-contained single chip smart vision camera. The solution to this problem was found to correct the offset internally in the pixel itself without increasing the size of the pixel or sensor, and without needing any external memory or software overhead. The hot carrier degradation of MOS transistors which is normally considered as a detrimental effect in semiconductor devices is advantageously used. Degradation experiments indicate that to first

approach only threshold voltages are affected while the other transistor parameters such as the transconductance remain quite stable. This characteristic is used as a method to realize a homogeneous response for all the pixels as represented in figure 2. A high current density is loaded on e. g. the source follower transistor (13) or any other by applying strongly different voltages (17) and (16) and an appropriate voltage on (12). Taking programming voltages of 16V at (17), 9V for (12), 6V for (15) and 0V for (16), voltage shifts of 200 mV are realised in about 10 minutes. Figure 9 illustrates that the stress operation can be performed without flattening the logarithmic response curve. The relaxation effect that occurs after the stress operation makes it necessary to stress the pixel in consecutive iterations. In this way the non-uniformity of the response is reduced to the level of the temporal noise (<5mV p/p). As a result the pixel's threshold voltage will shift or degrade to a predetermined value. By repeating the operation for different pixels on different times, a pixel matrix with uniform response characteristics is obtained. One can also realize an analog non-volatile memory using this technique.

An imaging sensor as described hereabove can be used as an intelligent imager. Such imager can be achieved as an "imaging system on a chip" and is intended to be interfaced to the outside world without additional external circuiting or post processing.

For illustrating an application of this image sensor, its integration within a camera module, the "Fuga 15a" smart camera, is disclosed in figure 10.

An addressable imager with logarithmic response behaves like a 256 Kbyte ROM : after applying an X - Y address (x - y position in matrix), the pixel intensity is returned. The following features are integrated:

- total die size: 3.6 x 3.6 mm^2,
- 512 x 512 3-transistor pixels, pitch 6.6 μm,
- layer of dummy pixels around the active matrix,
- pixels have a continuous operation in time (non-integrating),
- logarithmic intensity to voltage conversion,
- extra column with reference current sources for calibration of the pixel photocurrents,
- output load 20 pF,
- addressing speed 4 Mhz (X), up to 500 kHz (Y),
- supply 3.0..3.3 V (operates also from 1.7 to 5 V - but behavior and lifetime not documented).

It is another object of the present invention to provide a CMOS image sensor having a color sensitivity. Therefore, a color mosaic filter is prepared and deposited on the pixel structure of the CMOS image sensor according to the present invention.

Such color mosaic filter preferably has the same structure as the pixel array structure of the CMOS image sensor. In order to achieve this structure, a mask set is used suited for the definition of the pixel structure of the CMOS image sensor and for preparing and depositing the color mosaic filter on the CMOS image sensor.

The process of preparing this color mosaic filter comprises at least the following steps:

- preparation of a color mixture in the form of a suspension, dispersion or solution containing at least polyvinyl alcohol, dichromat and the required pigment or dye
- spinning this color preparation on the pixel structure of the CMOS image sensor
- illuminating using a mask set suited for the pixel structure of the CMOS image sensor
- etching the illuminated part including rinsing and/or flashing steps.

The whole process may be repeated for depositing further colors.

In the above described embodiment the dichromat may be used as photosensitive agent or alternatively photoresist pay be used.

A preferred embodiment according to the above described process is as follows :

- preparation of the color mixture comprising 10 ml dye and 1 ml dichromat (0.35 g dichromat in 10 ml H_2O)
- spinning at 3000 rpm up to a thickness of 1.0 - 1.5 μm
- illuminating for a time period of 50 sec
- etching by rinsing with desionized water
- 30 sec oxygen plasma flashing (150 Watt).

Figure 11 describes a preferred embodiment of a method of fabrication of such color filter comprising the following steps:

1st color layer:

- 1st color mixture (blue) obtained as described hereabove
- spinning at 4000 t/min (step a)
- illumination without any mask during 50 sec

Spin on Glass (SOG) 314:

- spinning at 2500 t/min (step b)
- baking at 130°C for 20 hrs

Photo-lake XI500EL deposition:

- spinning at 4300 t/min (step c)
- pre-baked at 100°C for 15 min
- illumination with mask - 18 sec
- developing 351 - 1'10" (step d)
- full-baking at 110°C for 15 min

Etching SOG:

- CF4: 100 sccm
- Ar: 10 sccm
- 150 Watt - 240 sec (step e)

Etching the 1st color layer + deposition of a resist:

- O2: 10 sccm
- 150 Watt - 10 min (step f)

The preceding steps may be repeated to deposit further colors.

Claims

1. A pixel (100 or 500) structure for CMOS imaging applications, comprising:

   - a photosensitive element (10 or 50)
   - a load transistor (11 or 51) in series with the photosensitive element (10 or 50);
   - means comprising at least another transistor (13, 14 or 22, 23 or 32 or 53) coupled to said photosensitive element (10 or 50) and said load transistor (11 or 51) for reading out the signals acquired in said photosensitive element (10 or 50) and converting to a voltage drop across said load transistor (11 or 51), characterized in that the gate length of at least the load transistor (11 or 51) is increased by at least 10% compared to the gate length of the transistors manufactured according to the layout rules imposed by CMOS manufacturing process, whereby increasing the light sensitivity of said pixel structure.

2. A CMOS image sensor having a geometric configuration of pixels (100) consisting in a structure as claimed in claim 1, each pixel having at least one photodiode (10) and a load transistor (11) having its gate tied to a voltage (12) and wherein the read-out means comprise at least a second transistor which is an emitter follower (13) connected to a data read-out line (16).

3. A CMOS image sensor having a geometric configuration of pixel (100) consisting in a structure as claimed in claim 1, each pixel having at least one photodiode (10) and a load transistor (11) of which the drain is not tied to a voltage and wherein the read-out means comprise a second transistor (22) and a third transistor (23) which is acting as a switch and is connected to a data read-out line (26).

4. A CMOS image sensor having a geometric configuration of pixel (100) consisting in a structure as claimed in claim 1, each pixel having at least one photodiode (10) and a load transistor (11) and read-out means comprising only another transistor (32), said pixel being read-out in both X - Y, and Y - X modes.

5. A CMOS image sensor having a geometric configuration of pixels (500) comprising a structure as claimed in claim 1 characterized in that each pixel (500) includes only a photodiode (50) and a switch (52), the load transistor (51) and the readout means (53) being common for one unit of several individual pixels (500).

6. A CMOS image sensor as claimed in any one of the claims 2 to 5 characterized in that it further comprises at least one pseudopixel comprising a current source instead of a photodiode, in order to determine the absolute light intensity of the pixels.

7. A CMOS image sensor as claimed in anyone of the claims 2 to 6 characterized in that it further comprises defined groups of (n x m) pixels (70, 71, 72 ,73) yielding one output voltage signal, said output voltage signal being some kind of average or minimized value of the individual output voltage signals of non-defective pixels in one group.

8. A CMOS image sensor as claimed in any one of the claims 2 to 7 characterized in that it further comprises a mosaic color filter which has preferably the structure of the pixel array.

9. Device comprising an image sensor as claimed in anyone of the claims 2 to 8 with a corresponding peripheric circuitry characterized in that it comprises

   - a signal processing unit (83),
   - a control circuit (84, 85) to adjust the output voltage signal (80) of the pixels (100) or units of pixel (500) in the sensor (800) within the input voltage (82) range of said signal processing unit (83),

   thereby providing an automatic brightness control of said sensor.

10. Method for increasing the homogeneity of the image found in an image sensor as claimed in anyone of the claims 2 to 6 characterized in that it comprises the following steps:

    - selecting an individual pixel (100 or 500),
    - loading a high current density on one of the transistors (11, 13, 14 or 53) of one pixel for a time span, said time span being chosen to shift the threshold voltage of said transistor (11, 13, 14 or 53) to a predetermined value.

11. Method for the fabrication of a color filter to be deposited on a CMOS image sensor according to claim 8 comprising the following steps:

    - preparation of a color mixture in the form of a suspension, dispersion or solution containing at least polyvinyl alcohol, dichromat and the required pigment or dye
    - spinning this color preparation on the pixel structure of the CMOS image sensor
    - illuminating using preferably the same mask set as the one used for manufacturing the pixel structure of the CMOS image sensor
    - etching the illuminated part including rinsing and/or flashing steps

12. Method according to claim 11 wherein the processing steps as recited therein are repeated for further colors.

13. Use of anyone of the devices claimed in any one of the claims 1 to 9 or of the methods claimed in claim 10, 11, and 12 for manufacturing a vision camera.

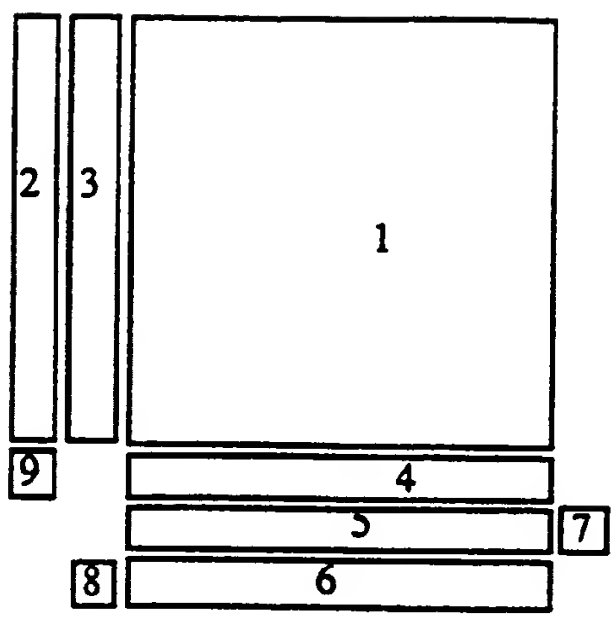

Fig.1

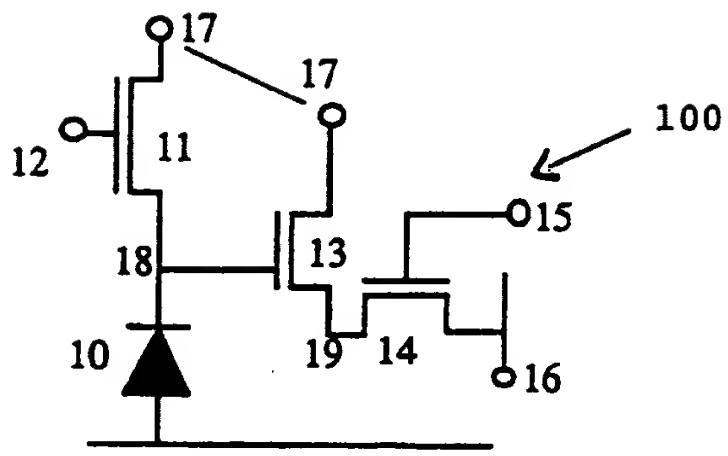

fig. 2

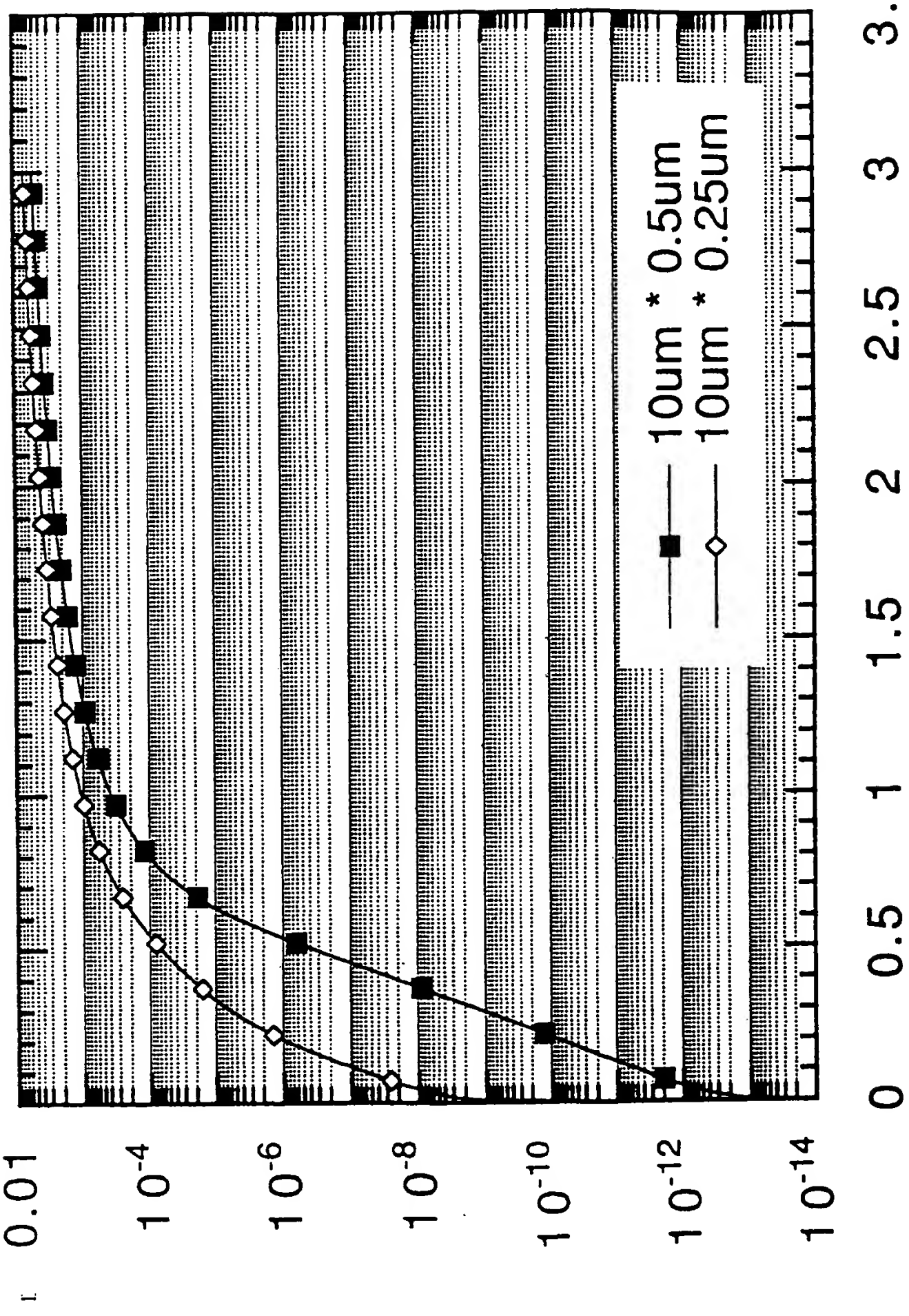
10um * 0.5um
10um * 0.25um
I
0.01
10-4
10-6
10-8
10-10
10-12
10-14
0
0.5
1
1.5
2
2.5
3
3.5
V

FIG. 3

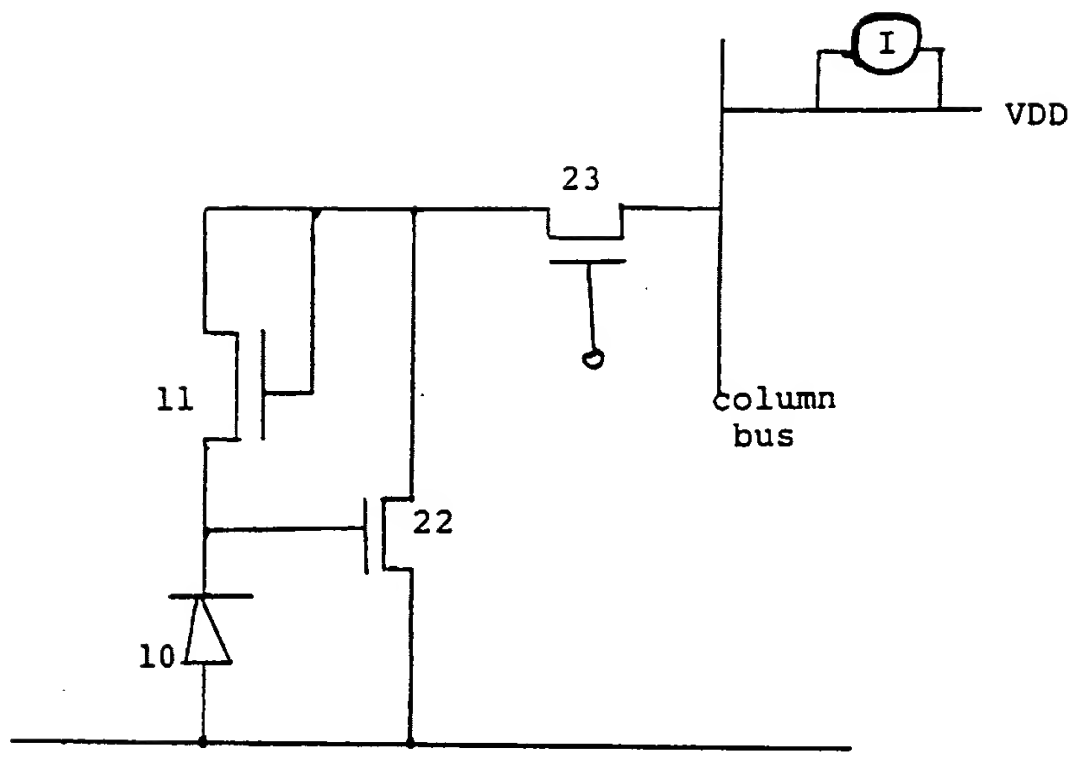

FIG. 4

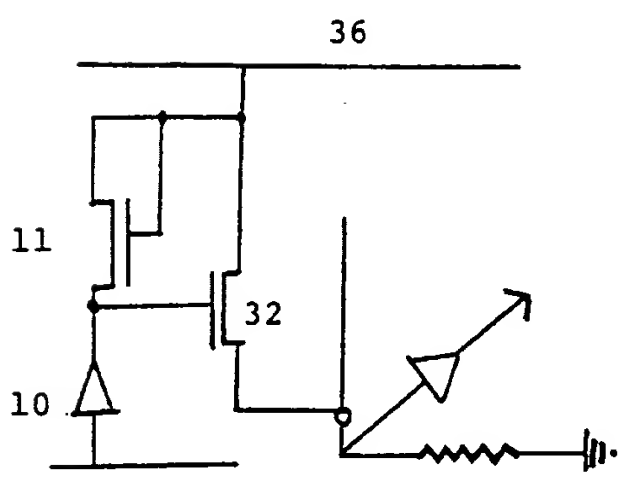

FIG. 5a

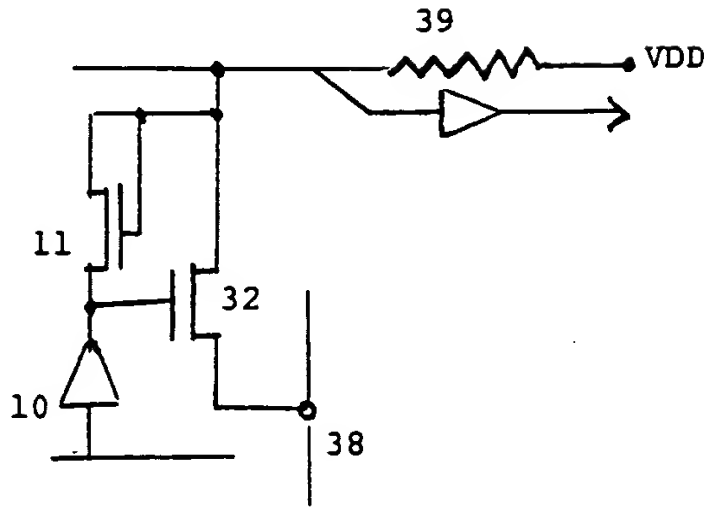

FIG. 5b

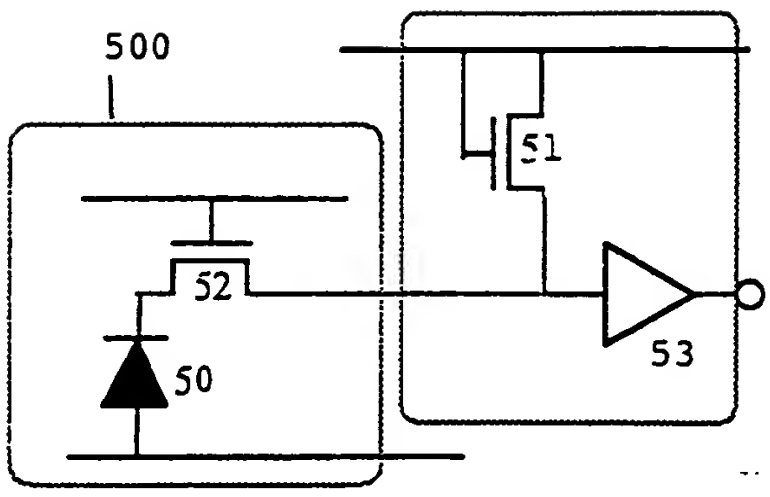

Fig. 6

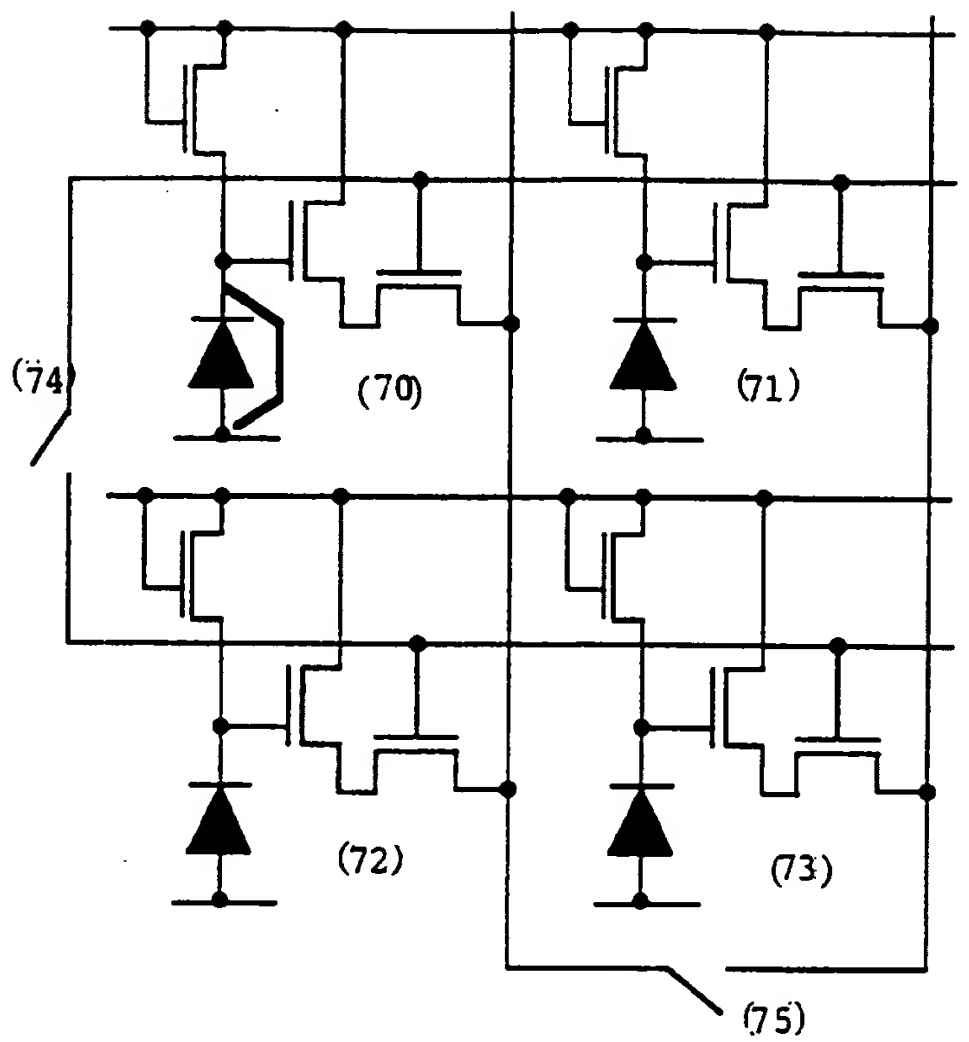

Fig. 7

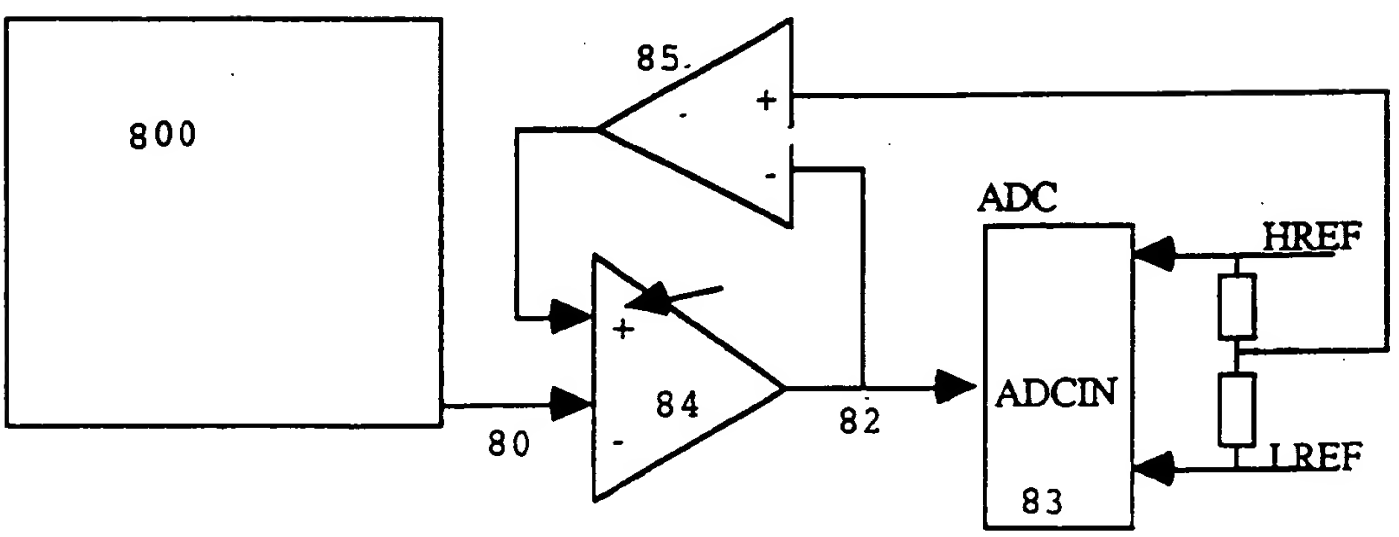

Fig. 8

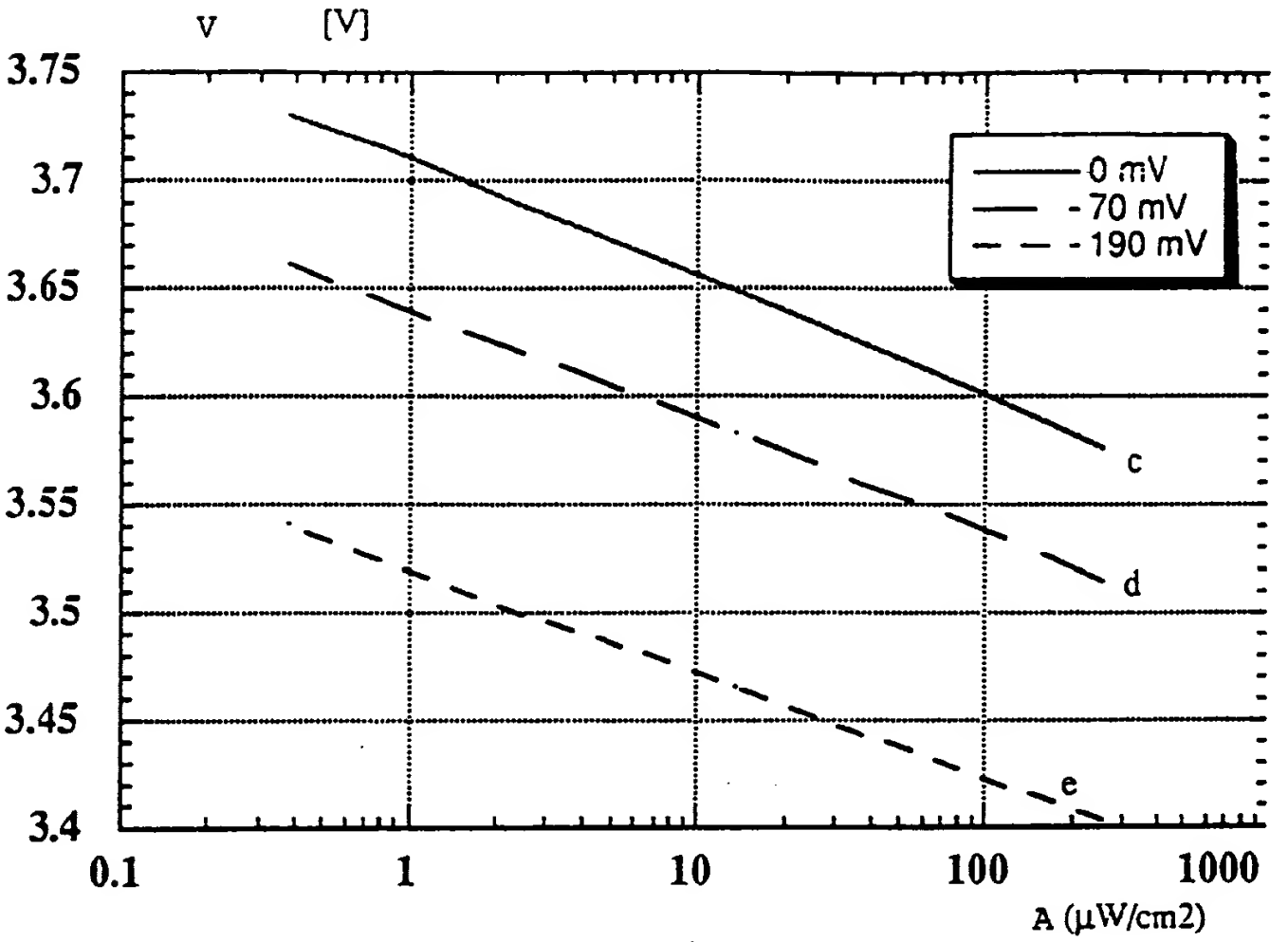
V [V]
3.75
3.7
3.65
3.6
3.55
3.5
3.45
3.4
0.1
1
10
100
1000
A (µW/cm2)
0 mV
- 70 mV
- 190 mV
c
d
e

Fig. 9

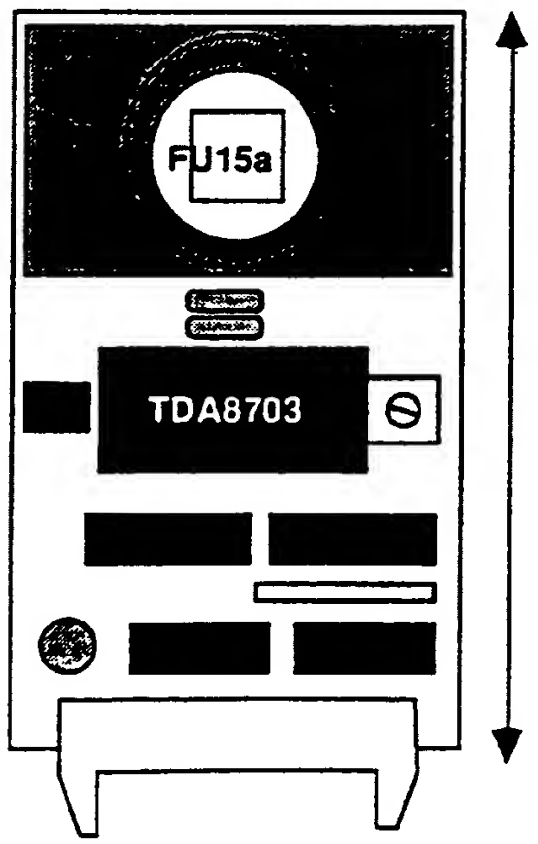
FU15a
TDA8703

Fig. 10

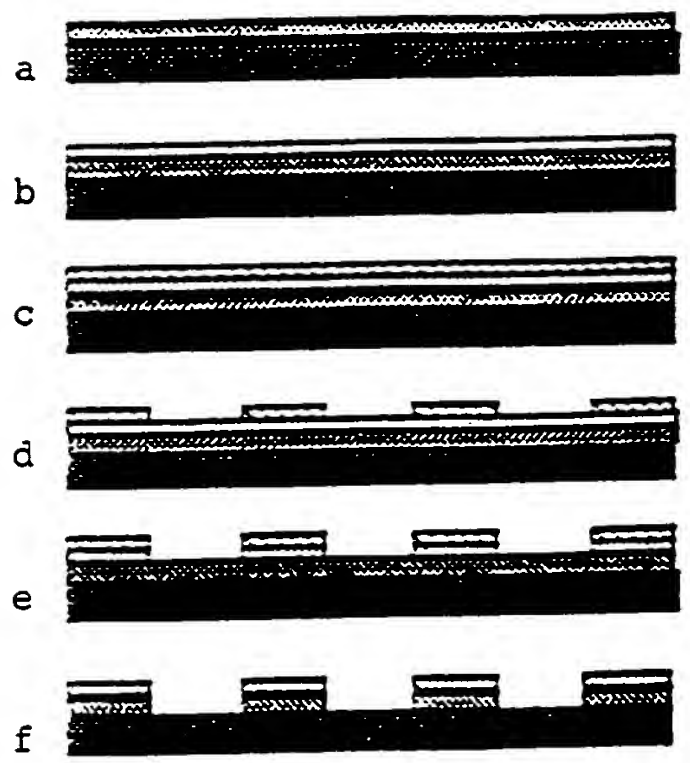

FIG. 11